**Shilpa Sunil Varaskar**

**Contact no:** 9820413541/ 9768176740 **email:** [varaskarshilpa@gmail.com](mailto:varaskarshilpa@gmail.com)

**Summary:**

I am an Electrical Engineer and a fresher seeking an opening in your esteemed organization where I will have an opportunity to work and learn under highly experienced professionals and upgrade my knowledge and skills in the field of engineering.

**Educational Qualifications:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Name of Examination** | **University/ Board** | **Name of College/ School** | **Year of passing** | **Percentage obtained** |
| M.E.  (Power Electronics and Drives) | University of Mumbai | Fr. C. Rodrigues Institute of Technology, Vashi | Currently appearing | FE  SGPI: 8.00 |
| B.E.  (Electrical Engineering) | University of Mumbai | Lokmanya Tilak College of Engineering, Koparkhairane, Navi Mumbai | June 2014 | 59.24% |
| H.S.C | Maharashtra Board | V.G Vaze College of Arts, Science and Commerce, Mulund | Feb 2010 | 77.50% |
| S.S.C | Maharashtra Board | Sri Ma Bal Niketan high School and Junior College, Thane | Mar 2008 | 84% |

**Computer skills:**

***Operating system***  Windows XP, Windows 7/8

***Packages*** Microsoft Office

***Software Tools***  Auto Cad, MATLAB

**Academic Projects:**

1. ***Name of Project:***  Finite Element Analysis of Transformer and its Optimization

***Project Description:*** The Project involves the modeling of transformer tank using

Pro-E, and its optimization based on the analysis results.

1. ***Name of Project:***  DC Source with Low Output Current Ripple

***Project Description:*** A DC source for low voltage high current applications is developed using Model Predictive Control. An interleaved dc-dc buck converter is simulated in MATLAB which even at high output current contains low ripples. This reduces unpredictable temperature rise, power loss and helps improve the life of electrolytic capacitors used in the circuit. Also a hardware model has been implemented using DSP.

**Co-curricular Activities:**

* Completed internship training at Siemens LTD, Kalwa in R&D (WSWB factory) during the period 15th June 2012 to 13th July 2012.
* Published a paper titled “A Comparative Simulation study of Buck Converter Topologies used in Low Ripple High Power Applications” at International Conference on Contours of Digital Technology (ICCDT), Mumbai in September 2015.
* Published a paper titled “Interleaved Buck Converter with Low Output Current Ripple using Model Predictive Algorithm” at International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS), Karpagam College of Engineering, Coimbatore in March 2016.

**Extra Curricular Activities:**

* Volunteered and participated in various events of Tech Zephyr organized at Lokmanya Tilak College of Engineering, Koparkhairane.
* Volunteered in Trantragyan event held at Lokmanya Tilak College of Engineering in March 2014.
* Secured several prizes in Drawing, Handwriting, 100m running and 4x100m Relay Competitions.

**Personal Details:**

***Date of birth***  February 27th, 1993

***Permanent Address*** 803, Morar Ashirwad CHS, Opp. Nitin Company,

Near Hotel Royal Challenge,

Thane (W), Maharashtra, Pin code: 400604

***Languages known*** English, Hindi, Marathi

***Hobbies*** Drawing, Travelling

**Marital Status** Unmarried

**My strengths:**

* Quick learner
* Smart worker
* Patience

**Shilpa Varaskar**